

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

## DESCRIPTION

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ) and clock-enable ( $\overline{CLKENAB}$  and  $\overline{CLKENBA}$ ) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select ( $\overline{SEL}$ ) input.

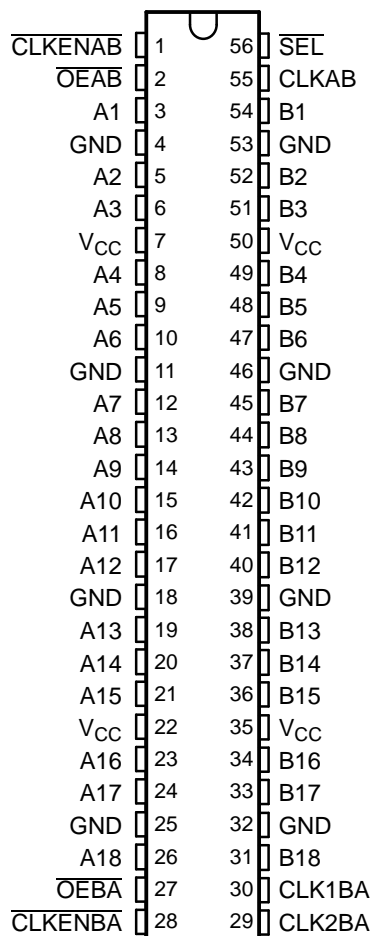
Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate  $\overline{CLKEN}$  inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16525 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**SN74ALVCH16525**  
**18-BIT REGISTERED BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES059E—NOVEMBER 1995—REVISED OCTOBER 2004

**FUNCTION TABLES**

**A-TO-B STORAGE**  
**( $\overline{OEAB} = L$ )**

INPUTS			OUTPUT B
$\overline{CLKENAB}$	CLKAB	A	
H	X	X	$B_0^{(1)}$
L	↑	L	L
L	↑	H	H

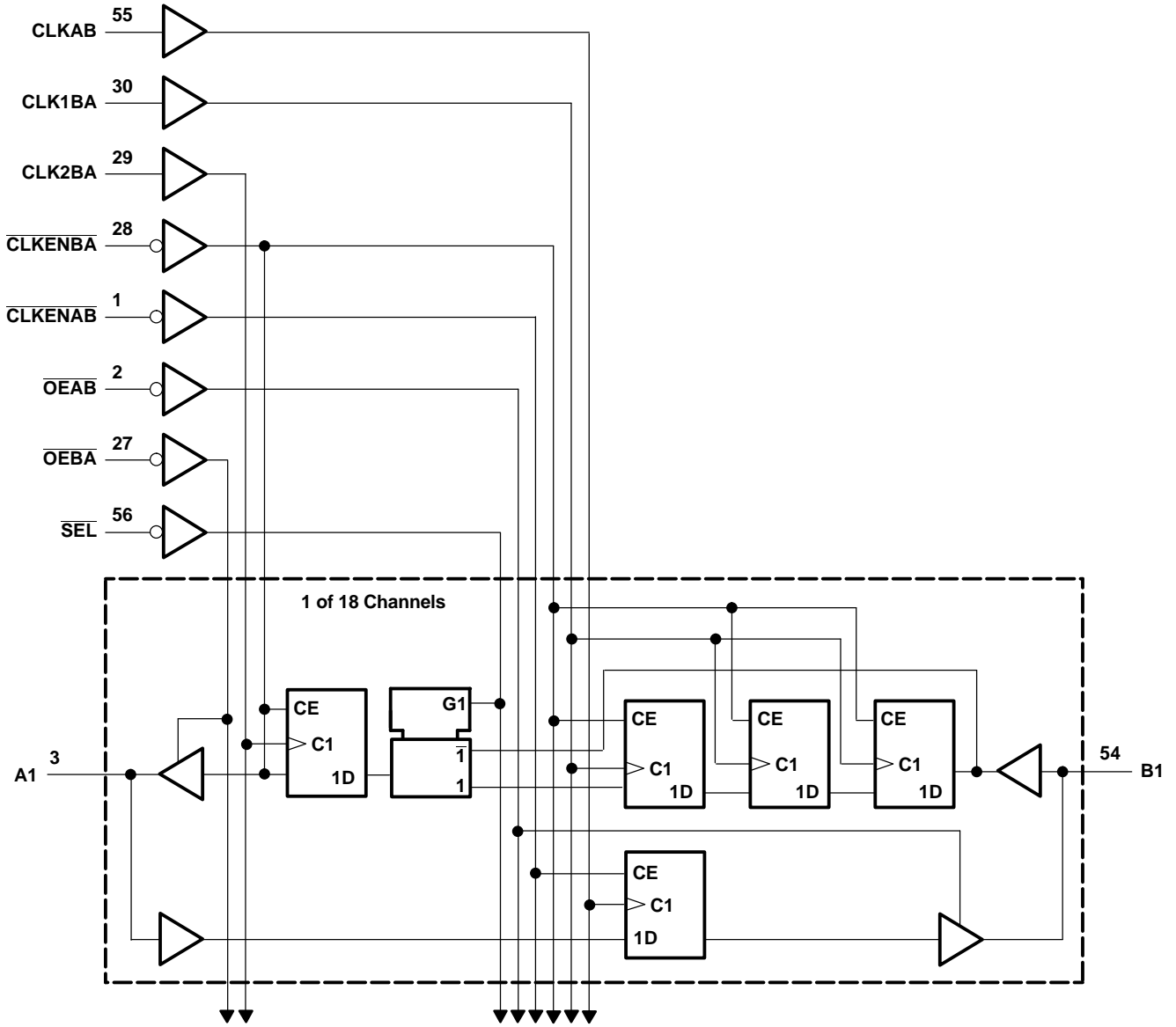
- (1) Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE**  
**( $\overline{OEBA} = L$ )**

INPUTS					OUTPUT A
$\overline{CLKENBA}$	CLK2BA	CLK1BA	$\overline{SEL}$	B	
H	X	X	X	X	$A_0^{(1)}$
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	$L^{(2)}$
L	↑	↑	L	H	$H^{(2)}$

- (1) Output level before the indicated steady-state input conditions were established  
(2) Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when  $\overline{SEL}$  is low.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN74ALVCH16525

## 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES059E–NOVEMBER 1995–REVISED OCTOBER 2004

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V	
V <sub>I</sub>	Input voltage range	Except I/O ports <sup>(2)</sup>		V	
		I/O ports <sup>(2)(3)</sup>			
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through each V <sub>CC</sub> or GND			±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		81	°C/W
		DL package		74	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		
		V <sub>CC</sub> = 2.7 V to 3.6 V		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		
		V <sub>CC</sub> = 2.7 V to 3.6 V		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		mA
		V <sub>CC</sub> = 2.3 V		
		V <sub>CC</sub> = 2.7 V		
		V <sub>CC</sub> = 3 V		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		mA
		V <sub>CC</sub> = 2.3 V		
		V <sub>CC</sub> = 2.7 V		
		V <sub>CC</sub> = 3 V		
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V	
	I <sub>OH</sub> = -4 mA	1.65 V	1.2				
	I <sub>OH</sub> = -6 mA	2.3 V	2				
	I <sub>OH</sub> = -12 mA		2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
I <sub>OH</sub> = -24 mA	3 V	2					
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.2			V	
	I <sub>OL</sub> = 4 mA	1.65 V	0.45				
	I <sub>OL</sub> = 6 mA	2.3 V	0.4				
	I <sub>OL</sub> = 12 mA		2.3 V	0.7			
			2.7 V	0.4			
	I <sub>OL</sub> = 24 mA	3 V	0.55				
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			μA	
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25			μA	
	V <sub>I</sub> = 1.07 V	1.65 V	-25				
	V <sub>I</sub> = 0.7 V	2.3 V	45				
	V <sub>I</sub> = 1.7 V	2.3 V	-45				
	V <sub>I</sub> = 0.8 V	3 V	75				
	V <sub>I</sub> = 2 V	3 V	-75				
	V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V	±500				
I <sub>OZ</sub> <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10			μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40			μA	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	750			μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3		pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7		pF	

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

# SN74ALVCH16525

## 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES059E–NOVEMBER 1995–REVISED OCTOBER 2004

### TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	(1)		120		125		150		MHz
$t_w$	Pulse duration, CLK high or low	(1)		3.2		3.2		3		ns
$t_{\text{su}}$	Setup time	A data before CLKAB $\uparrow$		(1)		1.3		1.3		ns
		B data before CLK2BA $\uparrow$		(1)		2.1		1.8		
		B data before CLK1BA $\uparrow$		(1)		1.3		1.2		
		$\overline{\text{SEL}}$ before CLK2BA $\uparrow$		(1)		3.3		3.3		
		$\overline{\text{CLKENAB}}$ before CLKAB $\uparrow$		(1)		2.1		1.9		
		$\overline{\text{CLKENBA}}$ before CLK1BA $\uparrow$		(1)		2.7		2.5		
$t_h$	Hold time	A data after CLKAB $\uparrow$		(1)		0.7		0.4		ns
		B data after CLK2BA $\uparrow$		(1)		0.4		0		
		B data after CLK1BA $\uparrow$		(1)		0.8		0.4		
		$\overline{\text{SEL}}$ after CLK2BA $\uparrow$		(1)		0		0		
		$\overline{\text{CLKENAB}}$ after CLKAB $\uparrow$		(1)		0.1		0.3		
		$\overline{\text{CLKENBA}}$ after CLK1BA $\uparrow$		(1)		0		0		
$\overline{\text{CLKENBA}}$ after CLK2BA $\uparrow$		(1)		0		0		0		

(1) This information was not available at the time of publication.

### SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			(1)		120		125		150		MHz
$t_{\text{pd}}$	CLKAB or CLK2BA	A or B		(1)	1	4.5	4.4		1	4.2	ns
$t_{\text{en}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B		(1)	1	6.1	6.1		1	5.1	ns
$t_{\text{dis}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B		(1)	1	6.3	5.4		1	4.9	ns

(1) This information was not available at the time of publication.

### OPERATING CHARACTERISTICS

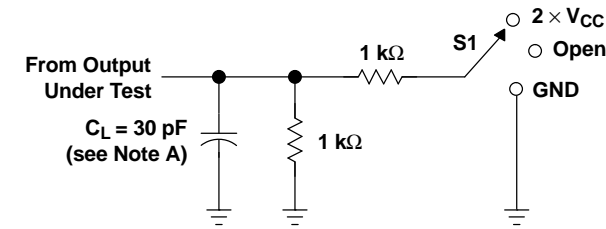
$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
$C_{\text{pd}}$	Power dissipation capacitance	Outputs enabled	(1)	160	160	pF
		Outputs disabled	(1)	160	160	

(1) This information was not available at the time of publication.

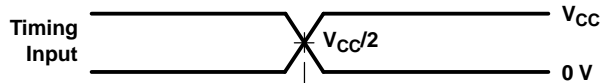
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$

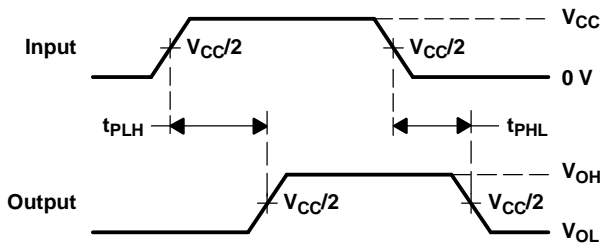


LOAD CIRCUIT

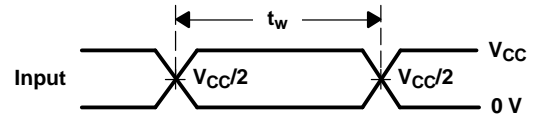
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



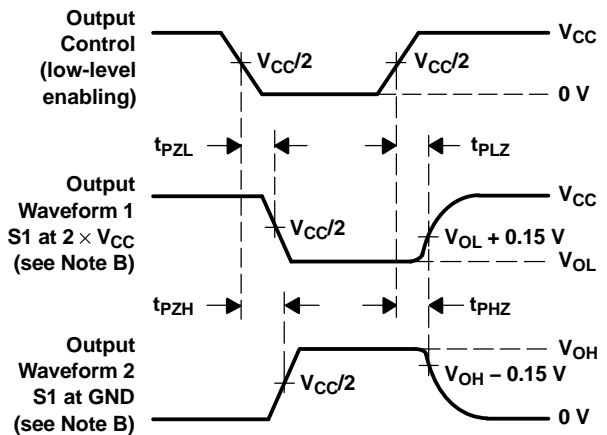
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



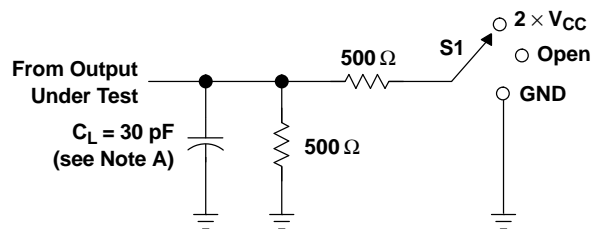
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

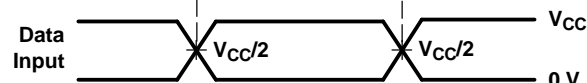
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

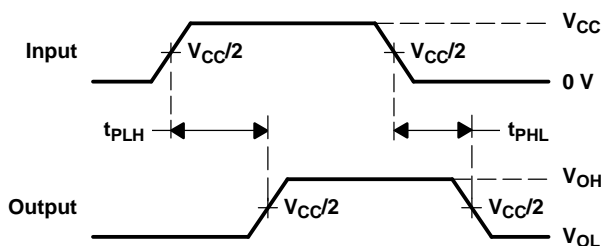


**LOAD CIRCUIT**

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



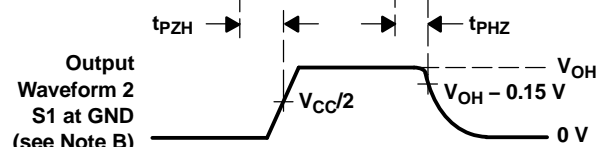
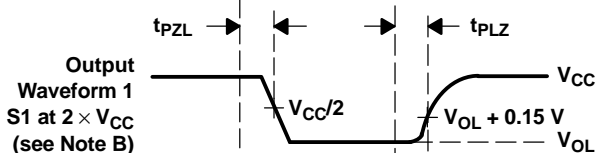
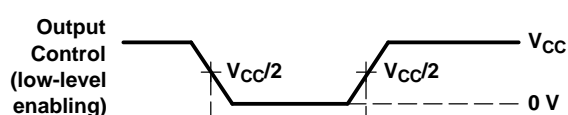
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

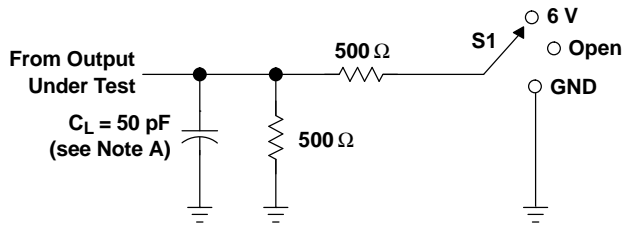
- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**



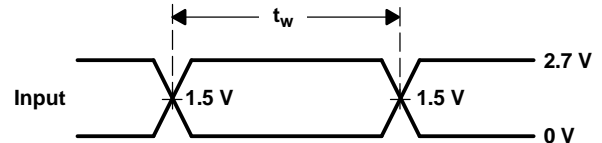
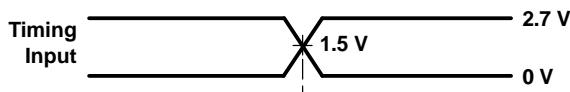
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

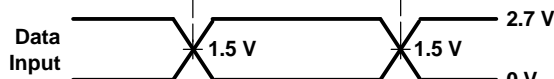


LOAD CIRCUIT

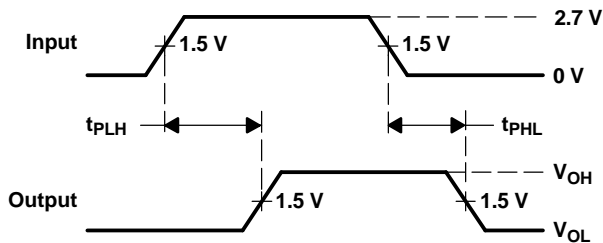
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



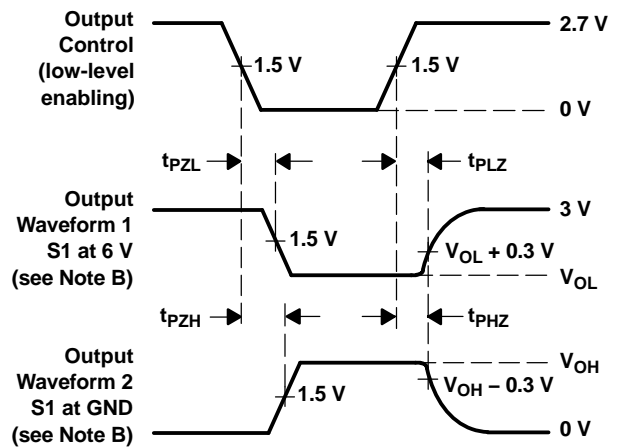
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
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 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ALVCH16525DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16525DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16525DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16525DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16525DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16525DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16525DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

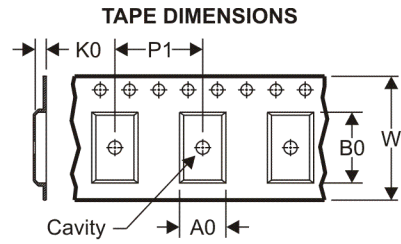
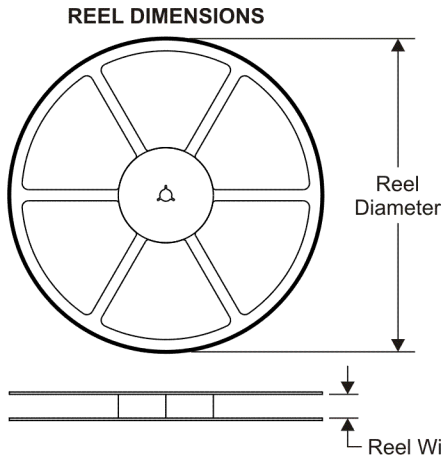
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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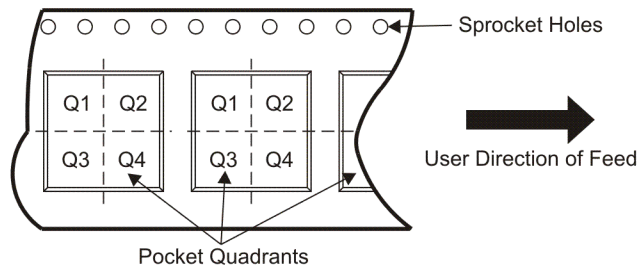
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**TAPE AND REEL INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16525DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16525DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16525DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16525DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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